Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S118	166	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) same (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 08:24
S122	144	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and "716"/$.ccls. and clock	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 08:44
S131	10	((redundant redundanc$3)near4(latch$3 register circuit gate cell macro)) near10 (reduc$3 eliminat$3 delet$3 remov$3 minimiz$3 optimiz$3)and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 08:54
S134	9	((redundant redundanc$3)same(latch$3 register circuit gate cell macro)) same (reduc$3 eliminat$3 delet$3 remov$3 minimiz$3 optimiz$3)same (domain)same clock	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 09:00
S138	281	(redundant redundanc$3)adj2(latch$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 09:16
S141	13	((redundant redundanc$3)near10(latch$3)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 09:21
S157	7	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") same (reduc$3 eliminat$3 remov$3 combin$3) same (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 15:55
S161	102	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") and (reduc$3 eliminat$3 remov$3 combin$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:00
S164	14	((redundant redundancy) adj2 (latch$3 circuit "flip flop " flip-flop")) and (reduc$3 eliminat$3 remov$3 combin$3) and (logical adj function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:03
S159	463	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") and (reduc$3 eliminat$3 remov$3 combin$3) and (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:08

S16 9	13	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") and (reduc$3 eliminat$3 remov$3 combin$3) and (clock adj cycle) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/02 16:11
S17 3	45	retiming same (redundant redundancy)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 08:26
S17 5	26	retiming same (redundant redundancy)and latch$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 08:27
S17 9	492	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 08:29
S18 2	16	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches gate circuit flip-flop "flip flop")and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/03 10:25
S18 1	236	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches gate circuit flip-flop "flip flop")and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 10:20
S19 6	16	(reduc$3 eliminat$3 remov$3) same (redundant redundancy)same (latch latches gate circuit flip-flop "flip flop")and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 10:24
S21 0	54	((redundant redundanc$3)adj2(latch$3)) and ("physical design" layout)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 15:53
S21 3	11	((redundant redundanc$3)near5(latch$3 register circuit gate cell macro)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and retiming and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:09
S21 8	29	((redundant redundanc$3)near5(latch$3 register)) and (reduc$3 eliminat$3 delet$3 remov$3 compact$3 compress$3 minimiz$3 optimiz$3) and "716"/$. ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:13
S16 7	133	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") same (reduc$3 eliminat$3 remov$3 combin$3) and (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:20

S22 1	47	(redundant redundancy) adj2 (latch$3 circuit "flip flop" " flip-flop") same (reduc$3 eliminat$3 remov$3 combin$3) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:23
S22 3	77	"716"/$.ccls. and retiming	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:42
S23 0	47	layout and(redundan$3 adj2 latch$2)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:46
S23 3	31	layout and (redundan$3)same latch$2 same transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/04 16:48
S27 3	22	latch same transition same clock same period same combin$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 08:04
S27 6	12	redundant same (latch flip-flop register)same transition same (clock period) same combin$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 08:07
S28 2	2528	clock adj domain	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:28
S29 2	124	redundant and (latch$3 flip-flop register)and transition and (clock period) and combin$3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:46
S29 3	82	redundant and (latch$3 flip-flop register)and transition and (clock period) and combin$3 and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:49
S29 4	10	redundant and (latch$3 flip-flop register)and transition and (clock period) and combin$3 and (clock adj domain) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:51
S29 8	3	redundant same (latch$3 flip-flop register)same transition and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:53
S30 1	115	(redundant redundancy)same (latch$3 flip-flop register)and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 09:57

S28 0	5861	latch same transition same (clock or period)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:35
S30 6	111	latch same transition same (clock or period) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:44
S28 1	5875	(group$3 or combin$3) adj6 latch	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:45
S30 8	507	S307 same transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 10:46
S31 8	51	layout same latch same optimiz$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 12:59
S32 0	9	layout and redundant same latch same optimiz$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 13:00
S32 7	20	(latch same transition) and (clock adj (period cycle))and (clock adj domain) and redundant	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 13:08
S33 2	22	(redund$3 adj2 latch$2) and transition and (clock adj cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 14:46
S33 8	62	(redund$3 adj2 (latch$2 flip-flop clocked-gate)) and transition and (clock cycle domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 15:46
S34 2	16	(redundant) adj2(latch$3 flip-flop gate circuit) and (clock adj domain)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/08 18:49
S36 5	24	(redundant redundancy) same (latch flip-flop) and transition and retiming and layout	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/09 12:28
S38 3	20	redundant same (latch flip-flop)and (minimiz$3 reduc$3 optimiz$3) and transition and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/09 14:21

S40 1	9	(latch flip-flop register) same (redundancy redundant) and clock adj2 transition and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/09 15:52
S41 8	3	(layout same optimiz$5) and redundan$4 adj (latch flip-flop register)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 08:58
S42 2	16	redundant adj2 (latch$3 flip-flop) and transition and (optimiz$3 compact$3)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 09:04
S44 2	54	physical same design same layout same latch	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 11:54
S44 9	79	design same layout same latch and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 12:00
S46 2	53	identify$3 same redundan$2 same latch	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2005/08/10 13:37
S47 1	1158	latch near4 collaps$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:23
S47 4	253939	S472 and S473	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:24
S47 3	593417	transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:24
S47 2	2427883	clock or period	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:24
S47 5	13	S474 and S471	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:37
S47 7	1	S474 and S471 and redundancy	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:38

S47 6	0	S474 and S471 and redundant	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/10 16:38
S48 7	83	logic same design same physical same layout same simulation	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/11 08:41
S50 2	24	latch same transition same layout same cycle	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/11 16:42
S50 5	61	latch same transition and layout and simulation and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/11 16:48
S57 8	128	selection same output same logic and "AND" and inverter and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:10
S58 3	3	selection adj logic same active adj output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:18
S58 5	32	selection adj logic same output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:21
S59 0	1	demultiplexor and inverter and ("AND" "and") and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:26
S59 1	16	selection adj logic and inverter and ("AND" "and") and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/16 11:30
S59 9	7	demultiplexor and logic and selection and gate and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:48
S61 1	825	latch near3 collaps$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:56
S61 4	2	S611 and S612	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:57

S61 5	594695	transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:58
S61 7	20356	S612 and S616	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:59
S61 6	20356	transition and clock adj (period cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:59
S61 2	58205	clock adj (period cycle)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 12:59
S61 9	594695	transition	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:00
S61 8	2431651	clock or period	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:00
S62 1	8	S611 and S620	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:01
S62 0	254493	S618 and S619	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:01
S62 3	5	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3) same (non-active nonactive inactive passiv$5) near5 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:30
S62 5	18	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3 de-mux$3) same (non-active nonactive inactive passiv$5 off non-operat$3 non-operatable nonoperat$3 nonoperatable inoperat$3 inoperatable) near5 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 13:49
S62 2	572	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3) same (non-active nonactive inactive passiv$5) near5 output	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 18:58

S62 4	18	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 mux$3 demux$3) same (non-active nonactive inactive passiv$5 off non-operat$3 non-operatable nonoperat$3 nonoperatable inoperat$3 inoperatable) near5 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 19:03
S63 5	39	(latch flipflop FF ff register) same (select$3 multiplex$3 demultiplex$3 de-multiplex$3 mux$3 demux$3 de-mux$3) same (non-active nonactive inactive passiv$5 off non-operat$3 non-operatable nonoperat$3 nonoperatable inoperat$3 inoperatable) near10 output and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/08/17 19:12